

MECE336– Microprocessors I

Lecture 4 – Input/Output Ports

Associate Prof. Dr. Klaus Werner Schmidt

Department of Mechatronics Engineering – Çankaya University

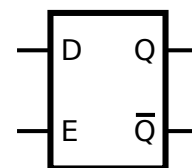
Compulsory Course in Mechatronics Engineering
Credits (3/2/4)

Course Webpage: <http://MECE336.cankaya.edu.tr>

Buffers: Latch and Tri-state Buffer

Latch (Flip-flop)

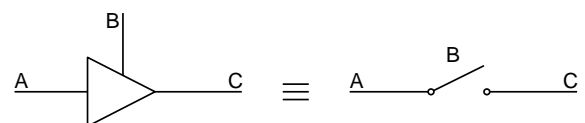
- Basic storage element in sequential logic that stores one bit of data
- Two stable states: 0 and 1
- Signal at D is stored in output Q if input E is 1



E/C	D	Q	\bar{Q}
0	X	Q_{old}	\bar{Q}_{old}
1	0	0	1
1	1	1	0

Tri-state Buffer

- Output port assumes high impedance if input B is 0
→ Multiple circuits can share the same output line
- Output port C has value of input A if input B is 1



A	B	C
X	0	Z (high impedance)
0	1	0
1	1	1

Overview: Peripherals

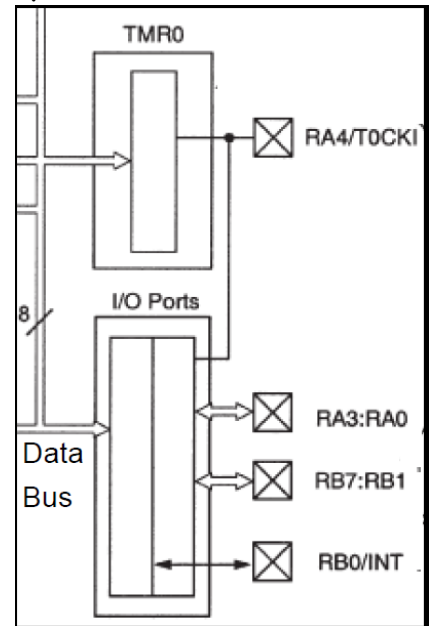
Port A

- General purpose 5-bit bi-directional port
- Separation of pins
 - pin RA0–RA3
 - pin RA4
- Additional functionality at pin RA4: Timer0

Port B

- General purpose 8-bit bi-directional port
- Separation of pins
 - pin RB0–RB3
 - pin RB4–RB7
- Additional functionality at pin RB0: Interrupt

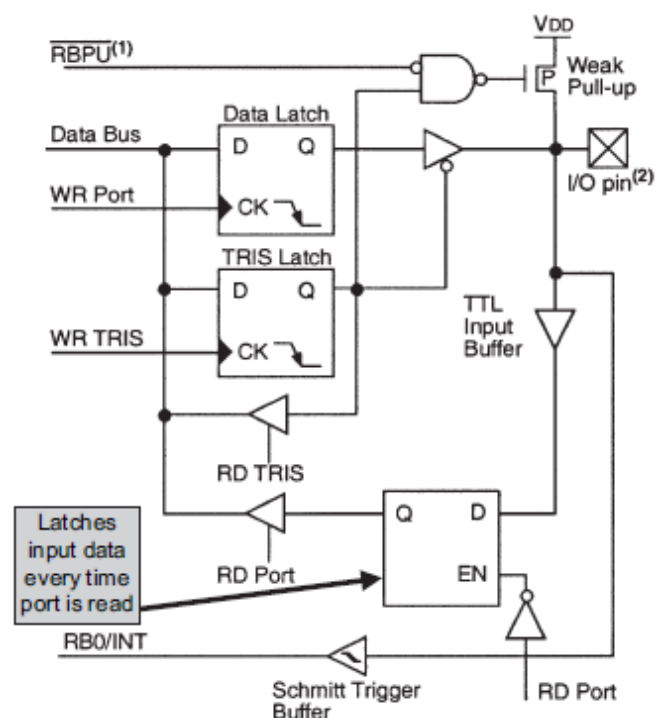
I/O Ports



Port B: Pin RB0 to RB3

Description

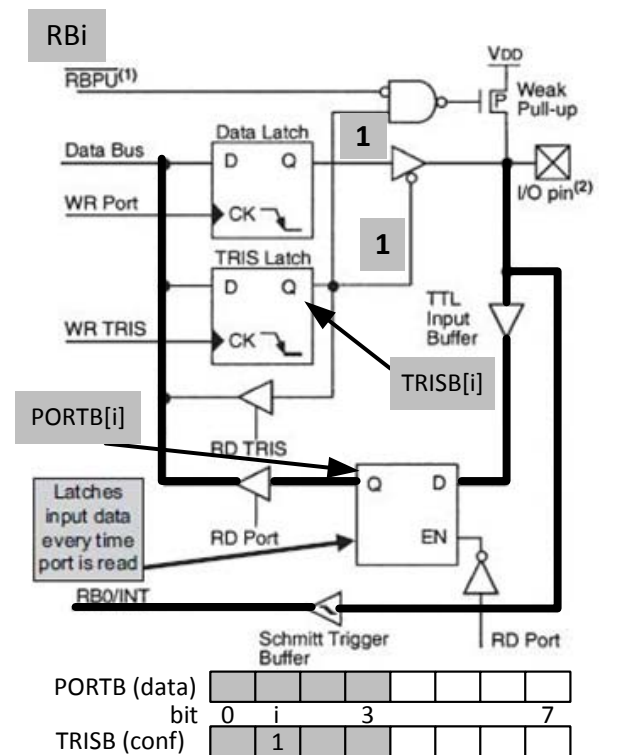
- Data Latch holds data value
 - Write data: trigger WR Port
 - Read data: trigger RD Port
- Direction in TRISB register
 - Value 1: input
 - Value 0: output
- Write TRIS: trigger WR TRIS
- Read TRIS: trigger RD TRIS
- Latch for input data
- Schmitt trigger for RB0
- Weak pull-up resistors for input operation



Port B: RB0 to RB3 – Input Operation

Description for Pin RBi

- Pin RBi as input
 - TRISB register bit i is 1
 - Output of TRIS latch is 1
⇒ Tri-state buffer at output is disabled
- Input value is latched during data read (RD Port is 1)
- Use weak pull-up: clear bit **RBPU** in the **OPTION** register



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Port B: Schmitt-Trigger at RB0/INT

Operation

- Special logic gate input that "cleans up" a corrupted logic signal
- When output signal is logic 0, the input signal has to pass the *positive going threshold* to obtain logic 1
- When the output signal is logic 1, the input signal has to pass the *negative going threshold* to obtain logic 0
⇒ small fluctuations in the input signal do not change the logic level

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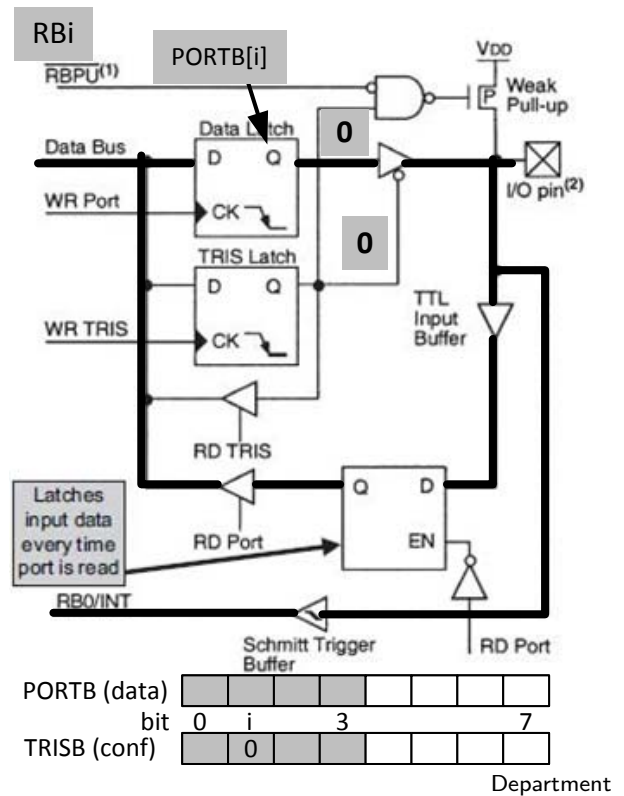
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Port B: RB0 to RB3 – Output Operation

Description for Pin RBi

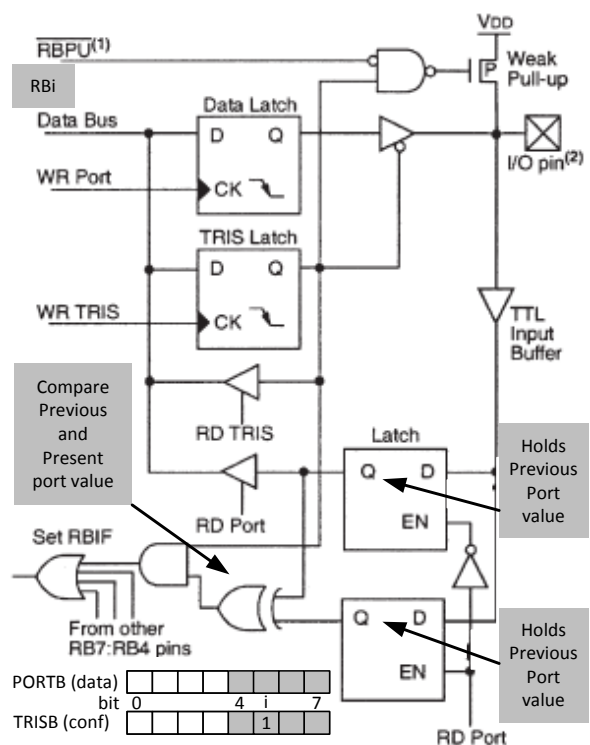
- Pin RBi as output
 - TRISB register bit i is 0
 - Output of TRIS latch is 0
 - ⇒ Tri-state buffer at output is enabled
 - ⇒ Weak pull-up is disabled
- Direct transfer of data latch value to output pin



Port B: RB4 to RB7

Description for Pin RBi

- Same functionality as Port RB0–RB3
- Additional functionality: Data value from previous read operation is stored in second latch
 - ⇒ An interrupt can be generated if the data value changes



Port B: Programming

Configuration: TRISB register Explanation

- TRISB on memory bank 1

```
status equ 03
bsf     status,5
```

- Write configuration to TRISB

```
movlw B'00000101'
movwf trisb
```

Data Value PORTB

- PORTB on memory bank 0

```
bcf     status,5
```

- Write value to Port B

```
movlw B'10100010'
movwf portb
```

Port B: Electrical Input Connections

Single-Pole Double-Throw (SPDT) Schematic

- One terminal connected to ground
- One terminal connected to supply
- Switch selects one of the terminals

Single-Pole Single-Throw (SPST)

- Pull-up resistor connected to one terminal
- One terminal connected to ground

Port B: Electrical Output Connections

LED with Sourcing Current

- Positive LED pin is connected to gate via resistor
- Negative LED pin at ground
- Current flows out of the gate
- Compute resistor value depending on LED current requirements

Schematic

LED with Sinking Current

- Positive LED pin is connected to supply via resistor
- Negative LED pin at gate
- Current flows into the gate

Port B: Application Examples

Example

- Use one Port B pin as input pin and one Port B pin as output pin
- Connect one push-button to the input pin
- Connect one LED to the output pin
- Turn on the LED if the push-button is pressed

Circuit

Port B: Application Examples

Program

Port B: Application Examples

Example

- Use one Port B pin as input pin and two Port B pins as output pin
- Connect one push-button to the input pin
- Connect one LED to each output pin
- Turn on one LED if the push-button is pressed and the other LED if the push button is not pressed

Circuit

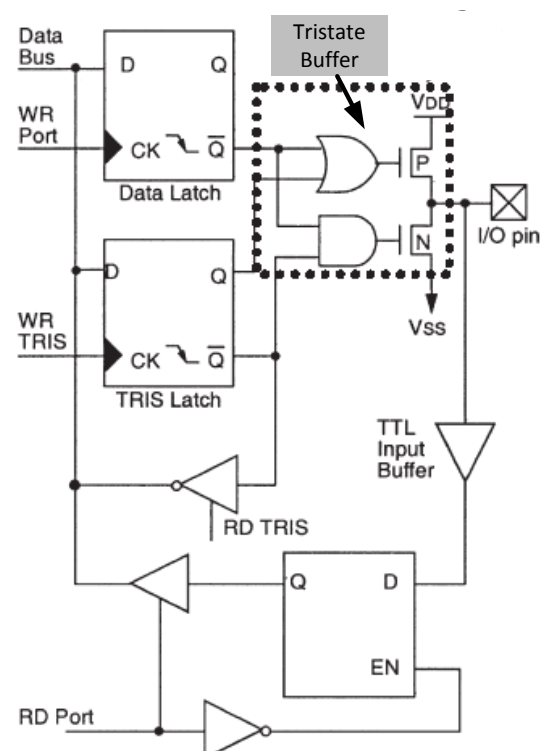
Port B: Application Examples

Program

Port A: RA0 to RA3 – General

Description

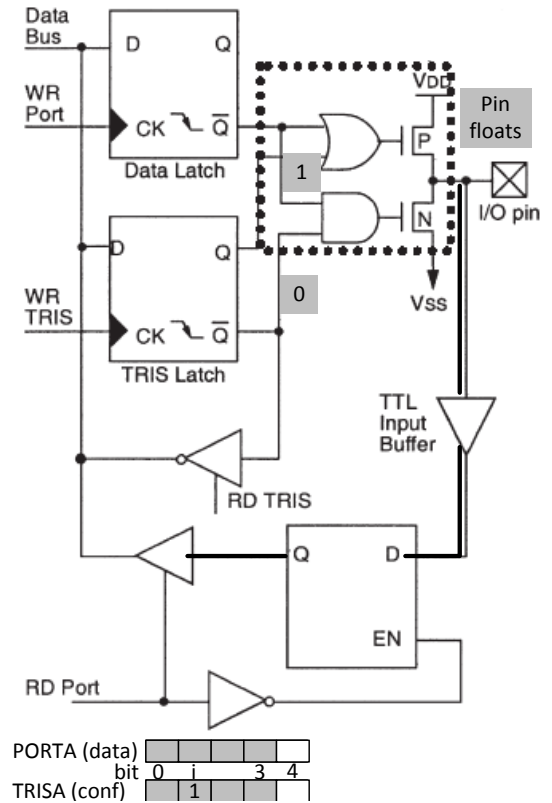
- Data Latch holds data value
 - Write data: trigger WR Port
 - Read data: trigger RD Port
- Direction in TRISA register
 - Value 1: input
 - Value 0: output
- Write TRIS: trigger WR TRIS
- Read TRIS: trigger RD TRIS
- Latch for input data
- Tri-state buffer for "open drain" output



Port A: RA0 to RA3 – Input Configuration

Description for Pin RA_i

- Pin RA_i as input
 - TRISA register bit *i* is 1
 - Output of TRIS latch is 1
 - Negated TRIS latch is 0
 - ⇒ Tri-state buffer is disabled
- Input value is latched during data read (RD Port is 1)

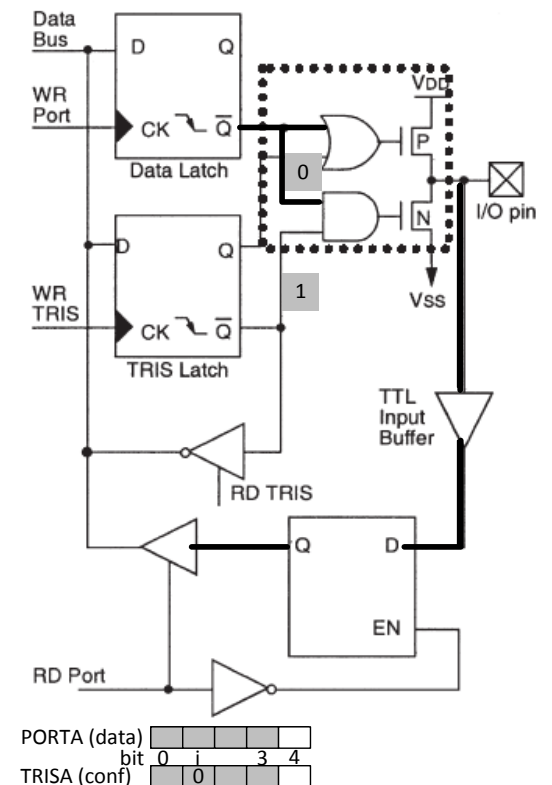


Port A: RA0 to RA3 – Output

Description for Pin RA_i

- Pin RA_i as output
 - TRISA register bit *i* is 0
 - Output of TRIS latch is 0
 - Negated TRIS latch is 1

⇒ Tri-state buffer provides data value at output



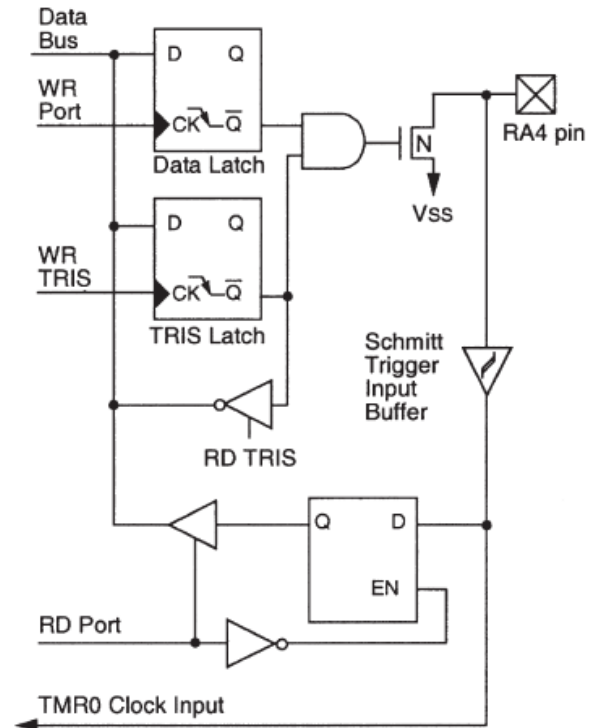
Port A: RA4

Description

- Pin RA4 as output
 - TRISA register bit 4 is 0
 - Output of TRIS latch is 0
 - Negated TRIS latch is 1

⇒ "Open drain" output is undefined for data value 1

⇒ Connect pull-up resistor to supply voltage



Port A: Programming

Configuration: TRISA register

- TRISA on memory bank 1

```
status equ 03
bsf status,5
```

- Write configuration to TRISA

```
movlw B'00000101'
movwf trisa
```

Data Value PORTA

- PORTA on memory bank 0

```
bcf status,5
```

- Write value to Port A

```
movlw B'10100010'
movwf porta
```

Explanation

Port A: Application Examples

Example

- Connect one push-button to an input pin at Port A
- Turn on a LED at a Port A pin if the push-button is pressed
- Turn on a LED at a Port B pin if the push-button is not pressed

Circuit

Port A: Application Examples

Program

Port A: Application Examples

Program

