Laboratory 5: Clock and Delays

Problem 7:

Write and compile the following program in MPLAB. Simulate your program step by step and observe the signal at RB0 using the logic analyzer view (from Window→Simulator→Analyzer).

```
1   list p=16f84a;
2   include "p16f84a.inc";
3   __config _CP_OFF&_WDT_OFF&_XT_OSC;
4   org 0;
5   main;
6   clrf PORTB;
7   bsf STATUS, RP0;
8   clrf TRISB;
9   bcf STATUS, RP0;
10  bsf PORTB,0;
11  nop;
12  nop;
13  nop;
14  nop;
15  bcf PORTB,0;
16  end;
```

Problem 8:

a. Write a delay loop as in the lecture with $k = 2$ and $N = 10$ in MPLAB. Turn on RB0 before the delay loop and turn of RB0 after the delay loop. How many instruction cycles are there in the delay loop?

b. Simulate your program step by step and observe the signal at RB0 using the logic analyzer view. How many instruction cycles do you count between RB0 = 1 and RB0 = 0?

c. What is the delay for the oscillator frequencies 100 kHz, 500 kHz, 4 MHz, 20 MHz?

Problem 9:

We want to realize a delay of 0.6 s for an oscillator frequency of 4 MHz.

a. How many `nop` instructions would you need in a single delay loop?

b. Choose suitable values of k_1, k_2, N_1, N_2 for a realization with two cascaded delay loops.

c. Write and compile a program for the delay with two cascaded delay loops in MPLAB.

d. Observe the number of instruction cycles of the delay using the logic analyzer view.
Hint: Set "Logic Analyzer Settings → Buffer Size" to 1000 000.